REMARKS

This paper is filed in response to the non-final Office Action mailed on August 5, 2004. Claims 1 and 7 have been amended; claims 1-2 and 4-14 remain pending.

In response to the Office Action, numerous amendments have been made to the specification. No new matter is added thereby and each amendment is supported by the specification as filed or the specification as filed in combination with the drawings.

Specifically, the amendment to pages 1 and 2 in the previous amendments to page 3 are all grammatical in nature and only address the description of the prior art. No new matter is added thereby.

With respect to the amendments made to page 4 of the specification, the amended paragraph beginning on page 4, line 10 refers to the novel aspect of the present invention as illustrated by the remaining portion 37a of the etching stop layer 37 as illustrated in Fig. 3c and 3e. No new matter is added thereby.

The first two amendments made to page 5 are either grammatical in nature or address informalities. Support for the amendment to the paragraph beginning on page 5, line 27 is provided by the specification as filed and Figure 3A.

Support for the amendments to page 6 is found in the specification as filed and in the figures. For that matter, most amendments to the specification include references to the Figures for support. All amendments are made for clarification purposes to make the specification consistent with the drawings as filed. Thus, no new matter is added thereby.

The amendments to the paragraph beginning on page 7, line 8 are grammatical and are fully supported by the specification as filed and Figures 3C-3E. Similarly, the amendment to the paragraph beginning on page 7, line 21 fully supported by Figure 3D and reference to Figure 3D is made in the amendment to this paragraph. Clearly, looking at Figure 3D, the void B is formed in the interlayer insulating layer 41.

Finally, the amendment to the paragraph beginning on page 9, line 5 simply corrects a typographical error as the etching stop layer 37a clearly surrounds the via hole 39 as illustrated in Figs. 3B and 3C-3E. Again, no new matter is added thereby.

Applicants respectfully submit that all rejections to the specification under 35 U.S.C. §112, first paragraph have been addressed. Applicants further respectfully request that if the Examiner sees the need to make any further amendments to the specification, that he telephone the undersigned and make such changes by Examiner's amendment.

The Office Action also objects to claim 7. In response, claim 7 has been amended to traverse this rejection.

Next, the Office Action rejects claims 6-8 under 35 U.S.C. §112, first paragraph as allegedly failing to comply with the written description requirement. In response, Applicants present the following remarks.

Referring to the drawings as filed, Figure 3D clearly shows a void B formed in the fourth interlayer insulating layer 41. Referring to Figures 3C and 3D, it is clear that this void B is formed in the layer 41 during formation of the layer 41. Applicants admit that page 7, lines 27-28 of the specification as filed are unclear and that the language should have originally said "in the fourth interlayer insulating layer 41" instead of "in the via hole 39." While this mistake is regrettable, the language of amended claim 6 is clearly described by Figure 3D as filed and therefore the language of claim 6 is fully supported by the specification and drawings as filed. One skilled in the art would clearly realize that line 28 of page 7 of the application is a typographical error and that interlayer insulating layer 41 should have been substituted for via hole 39.

The rejection of claim 6 under 35 U.S.C. §112, first paragraph is therefore traversed and should be withdrawn.

Turning to the rejections based upon the prior art, the Office Action rejects claims 1-2, 4-5 and 9-14 under 35 U.S.C. § 103 as being unpatentable under U.S. Patent No. 6,093,632 ("Lin '632"), U.S. Patent No. 6,042,999 ("Lin '999") and U.S. Patent No. 6,180,514 ("Yeh"). In response, Applicants present the following remarks.

At the outset, under §§ 2142, 2143 of the MPEP:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP §§ 2142, 2143.

Applicants respectfully submit that no *prima facia* case of obviousness has been established because (1) no combination of Lin '632, Lin '999 and Yeh teaches or suggests *all* of the limitations of claim 1 and (2) there is no motivation or suggestion in these three references to make the many changes to Lin '632 that would be required to establish a *prima facia* case of obviousness.

Applicants respectfully submit that Lin '632 is deficient as a base reference for numerous reasons. In the chart below, claim 1 as presently amended is reprinted with the specific claim limitations not found in Lin '632 italicized and comments regarding Lin '632, Lin '999 and Yeh in the columns to the right.

Claim 1 (Previously Presented)	**Lin '632**	**Lin '999**	**Yeh**
A method for manufacturing multi-level interconnection lines of a semiconductor device comprising:			
forming a first interconnection line *in a second interlayer insulating layer* and a first etching stop layer sequentially formed on *a first interlayer insulating layer disposed on a semiconductor substrate*;	Lin '632 does not start with a construction that is formed on a first interlayer insulating layer. Instead, Lin '632, in Figure 7 and 8, clearly starts with vias and interconnect lines 2 formed in an insulating layer 1 which presumably is disposed on a substrate (not shown). Thus, Lin '632 is missing an equivalent to a first interlayer insulating layer upon which subsequent structures are built as recited in amended claim 1.	Lin '999 is directed toward a damascene process through dielectric layers 110, 130 not insulating layers.	Yeh's layers 213 and 215 are also dielectric layers.
forming a third interlayer insulating layer on the first interconnection line			

and the first etching stop layer;			
forming a second etching stop layer *on the third interlayer insulating layer*;	The second etching stop layer 10b of Lin '632 is formed on the second interlayer insulating layer 4, not a third interlayer insulating layer as recited by claim 1.	Lin does not teach the formation of a second etching stop layer on a third interlayer insulating layer. Lin '999 is directed toward dielectric layers.	Yeh does not teach or suggest the formation of a second etching stop layer on an insulating layer but only a first etching stop layer 214 upon a dielectric layer 213.
forming a via hole exposing the first interconnection line by selectively etching the second etching stop layer *and the third interlayer insulating layer*;	The Patent Office admits that Lin does not form a via hole through the second etching stop layer as required by amended claim 1. Lin does not teach or suggest this concept *at all.*	Lin '999 forms a via 145 through dielectric layers 110, 130 with a stop layer 120 sandwiched therebetween. Thus, Lin '999 does not teach a selective etching of its layer 120.	Yeh does not teach or suggest the formation of a via hole through its etching stop layer. Instead, the etching stop layer 214 is already patterned.
forming an etching stop pattern around an inlet of the via hole by selectively etching the second etching stop layer leaving a portion of the second etching stop layer around the inlet of the via hole and exposing a portion of the third interlayer insulating layer;	Thus, Lin '632 clearly does not teach or suggest forming an etching stop pattern around an inlet of a via hole.	Line '999 does not teach or suggest forming an etching stop pattern around the inlet of the via hole 145.	Yeh does not teach or suggest the formation of an etching stop pattern around any inlet of a via hole. Instead, the pattern 214 defines the lower portion of the inlet 216b as shown in Fig. 2F.
forming a fourth interlayer insulating layer on the portion of the second etching stop layer *disposed around the inlet of the via hole* and the exposed portion of the third interlayer insulating layer *and at least partially covering the via hole*;	Lin '632 clearly does not teach or suggest forming a fourth interlayer insulating layer (Lin '632 only has three such layers) over an etching stop layer disposed around the inlet of a via hole and at least partially covering the via hole. Lin '632 is completely silent on both of these concepts.	Lin '999 in no way teaches or suggests the formation of an interlayer insulating layer over an etching stop pattern that surrounds a via hole and at least partially covering a via hole. Lin '999 cannot supplement Lin '632 in this regard.	Yeh in now way teaches or suggests the formation of an insulating layer over an etching stop pattern and at least partially over a via hole as recited in amended claim 1.
forming a trench by selectively etching the fourth interlayer insulating layer to expose the portion of the second etching stop layer disposed around the via hole; and forming a	In Lin '632, the via and trench are formed together. See Fig. 7 and column 5, line 54 to column 6, line 8.	Lin '999 forms the trench by etching a BARC layer.	In Yeh, the via and trench are formed together. See Fig. 2F

conductive layer in the trench and in the via hole so that the conductive layer at least partially covers the portion of the second etching stop layer disposed around the inlet of the via hole.			

Lin '632 discloses a dual damascene process in which the upper trench and via hole are formed together in a two-stage etching process. As set forth in Lin '632 at column 5, line 54 to column 6, line 8, a first RIE cycle of widens the diameter of the upper trench 15b using the previously created opening 15a in the photoresist 14 as a mask. Simultaneously, the narrow lower via 12b is etched using the spacing 12a between the etched stop pattern 10b as a mask. Thus, the upper trench 15b and lower via 12b are etched simultaneously.

This is in stark contrast to the method of claim 1 which requires the lower via hole to be formed before the upper trench. Amended claim 1 also requires an etching stop pattern to be formed after the formation of a via hole and then the deposition of a fourth insulating layer on top of an etching stop pattern and at least partially covering the formed via hole. Lin '632 teaches none of these steps and instead teaches away from claim 1 by forming the etching stop pattern before the lower via is formed. While Lin teaches a similar structure, Lin in no way teaches or suggests the method of claim 1 for arriving at such a structure. Thus, Lin is clearly deficient as a base reference.

In an attempt to supplement Lin '632, the Patent Office relies upon Lin '999 and Yeh. However, as shown above, these two references do not teach or suggest the missing elements of Lin '632. Lin '999 is directed toward a dual damascene process in dielectric layers, not insulating layers. Further, Lin '999 teaches nothing about forming an etched stop pattern around an inlet of a via hole and then depositing a fourth interlayer insulating layer on top of the etched stop pattern and at least partially covering the lower via hole. In Figure 2b of Lin '999, the via 145 extends through the dielectric layer 130, the etched stop layer 120, which is not patterned, and the lower dielectric layer 110. Then, the entire via 145 is filled with a BARC layer 150. There is no teaching or suggestion of depositing any insulation layer on the etched stop layer 120 or any layer that partially covers the via 145.

Similarly, Yeh does not teach or suggest this concept either. Yeh teaches away from claim 1 as Yeh's upper trench and lower via are formed simultaneously (see figures 2E, 2F), just like Lin '632.

Therefore, the obviousness rejection does not establish a *prima facia* case of obviousness for at least two reasons. First, the combination of prior art references do not teach or suggest all the claim limitations. Further, there is no suggestion or motivation in any of the three references to modify the procedure of Lin '632 in such a radical way so as to make Lin '632 conform with amended claim 1. This is because neither of the secondary references, Lin '999 or Yeh, teach or suggest the missing limitations of Lin '632. The only way to reconstruct amended claim 1 from these three references is to use impermissible hindsight.

Accordingly, Applicants respectfully submit that the obviousness rejection of claims 1-2, 4-5 and 9-14 is improper and should be withdrawn.

Finally, claims 6-8 stand rejected under 35 U.S.C. § 103 as being unpatentable over Lin '632, Lin '999, Yeh and further in view of U.S. Patent No. 6,737,350 ("Akahori").

The deficiencies of Lin '632, Lin '999 and Yeh are discussed above. Akahori is cited for the proposition that it teaches the formation of a layer 4, 111 over a via 31. The trench 41 is formed using a CF film having a low dielectric constant. The via hole 31 is formed by etching the silicon dioxide layer 3. After that etching, the etching stop layers 81, 82 are formed on the etched surface of the silicon dioxide layer 3. See Fig. 2d and 3a. Thereafter, the CF film 4 is deposited on top of the etching stop layers 81, 82 and is not embedded in the via hole 31.

Thus, the etching stop layers 81, 82 are formed after the formation of the via 31. At column 5, lines 50-55, Akahori states that the CF film 4 is deposited so that it grows inwardly as shown in Fig. 7. However, as shown in Fig. 7b, the film 4 completely covers the via 31 without a void as required by amended claim 6. Therefore, the CF film 4 of Akahori does not satisfy the limitation of being a fourth interlayer insulating film as required by amended claim 1 and it does not satisfy the requirement of a void formed therein as required by claim 6.

Akahori cannot supplement the other three references in that it does not teach or suggest the formation of a fourth interlayer insulating film that covers an etching stop pattern (the etching stop pattern is completely missing in Akahori) that surrounds the inlet of a via hole in that it at least partially covers the via hole as required by claims 1 and 6.

Therefore, Akahori in combination with Lin '632, Lin '999 and Yeh fails to teach or suggest every claim limitation of amended claim 1 or claim 6 and therefore no combination of these four references establishes a *prima facia* case of obviousness as required by §§ 2142 and 2143. Applicants respectfully submit that the obviousness rejection of claims 6-8 is improper and should be withdrawn.

With all objections having been addressed and traversed, Applicants respectfully submit that this application is in a condition for allowance and an early action so indicating is respectfully requested. Again, if the Examiner has any further changes that he thinks should be made to the specification, he is implored to telephone the undersigned to make these changes by Examiner's amendment. The undersigned is more than willing to work with the Examiner to expedite the allowance of this application.

The Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 13-2855.

Respectfully submitted,

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